**What is Claimed is:**

1. A method for manufacturing a stacked gate structure, the method comprising the steps of:

a ) sequentially forming a dielectric layer, a poly-silicon layer, a metal layer, a barrier layer, and a tungsten layer on a semiconductor substrate;

b) performing a rapid thermal annealing (RTA) process and thereby forming a silicide layer as a result of the reaction between said metal layer and said poly-silicon layer; and

c) patterning said tungsten layer, said barrier layer and said silicide layer and said poly-silicon layer to form said stacked gate structure.

2. The manufacturing method as claimed in claim 1, wherein said metal layer is made of metal selected from a group consisting of titanium, cobalt, nickel, platinum, tungsten, tantalum, molybdenum, hafnium and niobium.

3. The manufacturing method as claimed in claim 1, wherein said barrier layer is made of metal nitride selected from a group consisting of WN, TaN, and TiN.

4. The manufacturing method as claimed in claim 1, wherein, said rapid thermal annealing process is performed in a nitrogen ambient.

5. A method for manufacturing a stacked gate structure, the method comprising the steps of:

a) sequentially forming a dielectric layer, a poly-silicon layer, a metal layer, a barrier layer, and a tungsten layer on a semiconductor substrate;

b) patterning said tungsten layer, said barrier layer, said metal layer, and said poly-silicon layer to form said stacked gate structure; and

c) performing a rapid thermal annealing (RTA) process and thereby forming a silicide layer as a result of the reaction between said metal layer and said poly-silicon layer.

6. The manufacturing method as claimed in claim 5, wherein said metal layer is made of metal selected from a group consisting of titanium, cobalt, nickel, platinum, tungsten, tantalum, molybdenum, hafnium and niobium.

7. The manufacturing method as claimed in claim 5, wherein said barrier layer is made of metal nitride selected from a group consisting of WN, TaN, and TiN.

8. The manufacturing method as claimed in claim 5, wherein said rapid thermal annealing process is performed in a nitrogen ambient.

9. A method for manufacturing a field effect transistor, the method comprising the steps of:

a ) sequentially forming a dielectric layer, a poly-silicon layer, a metal layer and a barrier layer, and a tungsten layer on a semiconductor substrate;

b) performing a rapid thermal annealing (RTA) process and thereby forming a silicide layer as a result of the reaction between said metal layer and said poly-silicon layer ;

c) patterning said tungsten layer, said barrier layer and said silicide layer and said poly-silicon layer to form said stacked gate structure;

d) performing an ion implantation process, using said stacked gate electrode as a mask, to form spaced apart first source/drain regions in said semiconductor substrate;

e) forming a sidewall spacer adjacent to said stacked gate structure; and

f) performing another ion implantation process, using said sidewall spacer as a mask, to form spaced apart second source/drain regions of higher doping concentration than said first source/drain regions.

10. The manufacturing method as claimed in claim 9, wherein said metal layer is made of metal selected from a group consisting of titanium, cobalt, nickel, platinum, tungsten, tantalum, molybdenum, hafnium and niobium.

11. The manufacturing method as claimed in claim 9, wherein said barrier layer is made of metal nitride selected from a group consisting of WN, TaN, and TiN.

12. The manufacturing method as claimed in claim 9, wherein said rapid thermal annealing process is performed in a nitrogen ambient.

13. A method for manufacturing a field effect transistor, the method comprising the steps of:

a) sequentially forming a dielectric layer, a poly-silicon layer, a metal layer, a barrier layer, and a tungsten layer;

b) patterning said tungsten layer, said barrier layer, said metal layer, and said poly-silicon layer into said stacked gate structure;

c) performing a rapid thermal annealing (RTA) process, thereby forming a silicide layer as a result of the reaction between said metal layer and said poly-silicon layer;

d) performing an ion implantation process, using said stacked gate electrode as a mask, to form spaced apart first source/drain regions in said semiconductor substrate;

e) forming a sidewall spacer adjacent to said stacked gate structure; and

f) performing another ion implantation process, using said sidewall spacer as a mask, to form spaced apart second source/drain regions of higher doping concentration than said first source/drain regions.

14. The manufacturing method as claimed in claim 13, wherein said metal layer is made of metal selected from a group consisting of titanium, cobalt, nickel, platinum, tungsten, tantalum, molybdenum, hafnium and niobium.

15. The manufacturing method as claimed in claim 13, wherein said barrier layer is made of metal nitride selected from a group consisting of WN, TaN, and TiN.

16. The manufacturing method as claimed in claim 13, wherein said rapid thermal

annealing process is performed in a nitrogen ambient.